



Distinguished Lecture Series

# The Time-Triggered Architecture



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## Hermann Kopetz

Professor, Real-Time Systems,  
Vienna University of Technology, Austria

### Abstract

The time-triggered architecture (TTA), the result of more than twenty-five years of research in the domain of dependable real-time computing, provides a computing infrastructure for the design and implementation of dependable distributed embedded systems. A large real-time application is decomposed into nearly autonomous clusters and nodes, and a fault-tolerant global time base of known precision is generated at every node. In the TTA, this global time is used to precisely specify the interfaces among the nodes, to simplify the communication and agreement protocols, to perform prompt error detection, and to guarantee the timeliness of real-time applications. The TTA supports a two-phased design methodology, architecture design, and component design. During the architecture design phase, the interactions among the distributed components and the interfaces of the components are fully specified in the value domain and in the temporal domain. In the succeeding component implementation phase, the components are built, taking these interface specifications as constraints.

This talk presents the architecture model of the TTA, explains the design rationale, discusses the time-triggered communication protocols TTP and TTEthernet, and illustrates how transparent fault tolerance can be implemented in the TTA.

For more information: <http://www.iis.sinica.edu.tw/>

